ABSTRACT OF THE DISCLOSURE

A microprocessor apparatus is provided including multiple functional units, some of which can enter a power reduction mode to decrease overall power consumption when needed. The functional units generate respective activity signals to indicate the level of activity of each of the functional units. The activity outputs are monitored by utilization assessment logic to determine a current total power consumption value for the microprocessor. The microprocessor is capable of successively entering a series of power reduction modes when the current total power consumption value is greater than a threshold power value of a specified power profile.